IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

SOLAS OLED LTD.,

Plaintiff,

v.

SAMSUNG DISPLAY CO., LTD., SAMSUNG ELECTRONICS CO., LTD., AND SAMSUNG ELECTRONICS AMERICA, INC.,

Defendants.

Civil Action No. 2:19-cv-00152-JRG

[redacted]

DEFENDANTS SAMSUNG DISPLAY CO., LTD., SAMSUNG ELECTRONICS CO., LTD., AND SAMSUNG ELECTRONICS AMERICA, INC.'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

The constructions proposed by Defendants Samsung Display Co., Ltd., Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. reflect the meaning of the technical terms at issue to a person of ordinary skill in the art at the time of the invention based on the intrinsic evidence and, where applicable, extrinsic evidence showing a customary meaning. The parties have not disputed any term of U.S. Patent No. 6,072,450. As to U.S. Patent No. 7,446,338 ("the '338 patent"), Defendants' proposals represent the meaning of the terms in the context of the patent. Not only are Plaintiff Solas's constructions inconsistent with the intrinsic record, they contradict [redacted]—a fact Solas neglects to mention. The intrinsic evidence has not changed, and [redacted] belies many of its criticisms. Finally, as to U.S. Patent No. 9,256,311 ("the '311 patent"), the parties dispute a single term, with their dispute centering on the meaning of "edge." Defendants' proposal for this term represents the standard technical meaning of that term, as reflected in dictionaries.

II. LEGAL STANDARD

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (citation omitted). A person of ordinary skill "is deemed to read the claim term not only in the context of the particular claim . . ., but in the context of the entire patent, including the specification." *Id.* at 1313.

"The words of a claim are generally given their ordinary and customary meaning as understood by a person of ordinary skill in the art when read in the context of the specification and prosecution history." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012) (citing *Phillips*, 415 F.3d at 1313). A "term's ordinary meaning must be considered in the context of all the intrinsic evidence, including the claims, specification, and prosecution history."

Biogen Idec, Inc. v. GlaxoSmithKline LLC, 713 F.3d 1090, 1094 (Fed. Cir. 2013). When a patentee acts as his own lexicographer, or when a patentee disavows the full scope of a claim term in the specification or during prosecution, then the customary meaning does not apply. *See Trustees of Columbia v. Symantec Corp.*, 811 F.3d 1359, 1363-64 (Fed. Cir. 2016).

"[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Phillips*, 415 F.3d at 1315 (internal quotation marks omitted). Although extrinsic evidence can also be useful, it is "less significant than the intrinsic record." *Id.* at 1317 (internal quotation marks omitted). Courts have "especially noted the help that technical dictionaries may provide . . . to better understand the underlying technology and the way in which one of skill in the art might use the claim terms." *Id.* at 1318 (internal quotation marks omitted). Expert testimony may aid a court in understanding the underlying technology, but an expert's unsupported assertions as to a term's definition are not helpful to a court. *See id.*

III. ARGUMENT

A. Background of the '338 Patent

The '338 patent is directed to active-matrix organic electroluminescent (AMOLED) display panels. *See, e.g.*, Ex. 1 ('338 patent) at 1:17-21, 8:18-23. These are many-layered devices that consist of organic electroluminescent pixels and circuitry that drives the pixels to produce particular colors and brightness. Figure 6 is a cross-section illustrating the layered structure of an exemplary display panel of the '338 patent, consisting of these two main structures: (1) the red, green, and blue OLED pixels (Pr, Pg, and Pb), each made up of a pixel electrode 20a, an electroluminescent layer 20b, and a counter electrode 20c; and (2) the layers making up the "transistor array substrate" 50, *id.* at 10:42-47, which includes the transistors 21 and 23 that make up the active-matrix circuit for each pixel:

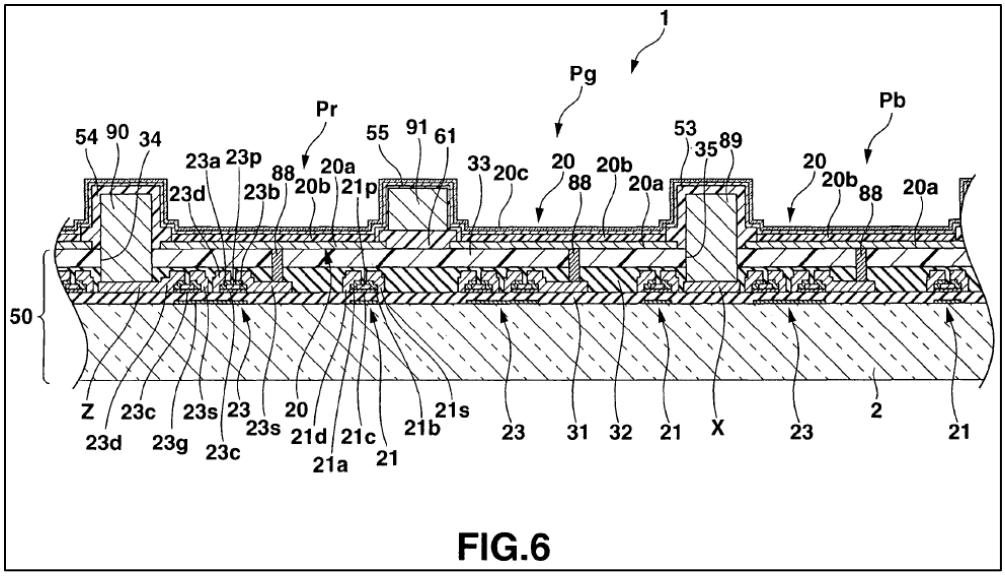

FIG.6

In the original patent application, original claim 1 was directed to the arrangement of elements in the layered structure, as exemplified by Figure 6. That claim, however, was rejected as anticipated by prior art. To overcome the rejection, the applicants amended claim 1, limiting it to a display having the particular three-transistor pixel circuit structure that had been recited in a dependent claim (original claim 2), illustrated in Figure 2 of the '338 patent. Ex. 2 at 2-3, 12. This circuit uses a current, called a write current, to set the brightness of each individual pixel. This current-controlled structure differed from circuits that used particular voltage signal levels applied to the gate of the driving transistor, rather than current, to control pixel brightness. *See* Ex. 1 ('338 patent) at 1:21-41 (describing that in a prior art reference, "a voltage of level representing the luminance is applied to the gate of the driving transistor through a signal line."). After the addition of this three-transistor circuit structure limitation, the claims of the '338 patent were allowed.

B. Disputed Terms of the '338 Patent[1]

1. "transistor array substrate" (claim 1)

[1] A person of ordinary skill in the art of the '338 patent would have had a relevant technical degree in electrical engineering, computer engineering, physics, or the like, and 2–3 years of experience in active matrix display design and/or manufacturing.

Defendants' Proposal	Plaintiff's Proposal
"a layered structure composed of a bottom insulating layer through a topmost layer on whose upper surface [pixel] electrodes are formed, which contains an array of transistors"	"layered structure upon which or within which a transistor array is fabricated"

The term "transistor array substrate" does not have a customary meaning in the art. It is a term specific to the '338 patent, and one which, as discussed below, the '338 patent defines as a layered structure composed of a bottom insulating layer through a topmost layer on whose upper surface electrodes are formed, which contains an array of transistors. Both the language of claim 1 and the specification support Defendants' proposal. Solas, in contrast, proposes a construction inconsistent with the claim language and the specification—and inconsistent with [redacted] Solas's vague proposal would also take a term clearly described in the claims and specification and render it indefinite.

The parties have two main disputes concerning this term: (1) whether the transistors are within the transistor array substrate; and (2) which of the many layers of a display panel constitute the transistor array substrate.

a. The transistors are contained in the transistor array substrate

Defendants' construction states that the transistor array substrate contains an array of transistors. In contrast, Solas proposes that the "transistor array substrate" need not contain an array of transistors. Solas's construction is contrary to the claim language and the specification.

The claim language recites "***a transistor array substrate*** which includes a plurality of pixels and ***comprises a plurality of transistors*** *for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain*." Ex. 1 ('338 patent) at 24:15-18 (emphasis added). The term "comprises" means "including but not limited to." *See, e.g.*, *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997). Thus, by the plain terms of the claim, the transistor array substrate must contain a plurality of transistors for each pixel (i.e., an array of

transistors). Moreover, the specification explains that the transistors are contained within the transistor array substrate. *See, e.g.*, Ex. 1 ('338 patent) at 10:45-47. Indeed, Solas's expert admits in his declaration that "[t]he transistor array substrate is a structure containing a transistor array." Dkt. 74-2 (Flasck Decl.) at ¶ 30.

Despite the clear requirement of the claim language, Solas's proposal ("layered structure *upon which or within which* a transistor array is fabricated") would permit the transistor array substrate to contain no transistors. Solas's expert admitted this in deposition:

> Q: . . . For the construction that you have offered for "transistor array substrate," which in paragraph 27 says, "layered structure upon which or within which a transistor array is fabricated," does that encompass . . . a layered structure in which none of the transistors are located within the transistor array?
>
> A: If there is a structure, a layered structure, and upon that layered structure there is a transistor array, then it would fall under this construction.
>
> Q: Even though none of the transistors were within the layered structure that [] is called the "transistor array substrate"?
>
> A: That's correct. . . .

Ex. 3 (Flasck Depo.) at 64:17-65:14 (objection omitted). This is contrary to the intrinsic evidence.

As stated in Defendants' proposal, the transistor array substrate is a "layered structure composed of a bottom insulating layer through a topmost layer on whose upper surface [pixel] electrodes are formed, *which contains an array of transistors*." Solas's contrary proposal is plainly inconsistent with the claim language and specification, and cannot be correct.

b. Solas's expert concedes that "transistor array substrate" does not have a customary meaning outside the '338 patent.

Having advanced a construction inconsistent with the clear intrinsic evidence, Solas attempts to support its proposal by claiming it represents an "ordinary and customary meaning" of "transistor array substrate," and arguing that departure from that purported plain meaning requires clear and unmistakable evidence. Dkt. 74 at 7-9. Solas's argument is meritless. *First*, although

Solas's brief attempts to portray its proposal as the plain and ordinary meaning of "transistor array substrate," Solas's expert conceded in deposition that the term does *not* have a customary meaning in the art. On the contrary, he testified that "transistor array substrate" may mean different things in different usages. Ex. 3 (Flasck Depo.) at 104:4-105:3 ("In one context this whole thing would be a transistor array substrate . . . in some contexts people would refer to a transistor array substrate as something less than this and generally would not include the electro-optical element. In this case it would not include the EL film . . . so I've seen it used both ways"), 57:5-7, 69:3-11.

Second, Solas does not cite any definition of the term "transistor array substrate." This belies its assertion that the term has an ordinary and customary meaning. Solas relies on an IEEE dictionary definition of a different term, "substrate." Ex. 3 (Flasck Depo.) at 69:17-19 ("Q. There is no IEEE definition for 'transistor array substrate," is there? A. I believe that is correct."). Solas's reliance on definitions of "substrate" is particularly inapt because the '338 patent distinguishes a "substrate" from "a transistor array substrate." *See, e.g.*, Ex. 1 ('338 patent) at 10:42-47 ("[T]he layered structure from **the insulating substrate 2** to the planarization film 33 is called a **transistor array substrate 50**") (emphases added). The patent teaches that an insulating substrate is just one portion of a transistor array substrate, which includes numerous other layers as well. *See id.*

Third, Solas's construction does not even match its dictionary definition, which says nothing of a structure being "layered." Ex. 3 (Flasck Depo.) at 73:11-74:10.

Thus, Solas cannot claim that its proposal represents the plain and ordinary meaning of "transistor array substrate." Rather, the language of the claims and the disclosures of the specification demonstrate that the meaning of that term is as Defendants propose—a proposal that matches *Solas's own* prior interpretation of that term (as discussed below).

c. The '338 patent defines which layers of an OLED display panel constitute the "transistor array substrate"

The claim language and the specification make clear that the "transistor array substrate" is a layered structure composed of a bottom insulating layer through a topmost layer on whose upper surface [pixel] electrodes are formed, as Defendants propose.[2]

First, the claim language supports Defendants' proposal. After reciting "a transistor array substrate," claim 1 proceeds to recite (1) that the interconnections "project from a surface of the transistor array substrate" and (2) "the pixel electrodes being arrayed along the interconnections between the interconnections *on the surface of the transistor array substrate*." Thus, according to the claim language, the pixel electrodes are "on the surface of the transistor array substrate," meaning that the "transistor array substrate" constitutes the layers up to but not including the pixel electrodes, as Defendants propose.

Second, consistent with the claim language, the specification discloses that the transistor array substrate constitutes the layers up to (but not including) the pixel electrode. The specification expressly states that "[t]he layered structure from the insulating substrate 2 to the planarization film 33 ***is called*** a transistor array substrate 50." Ex. 1 ('338 patent) at 10:45-47 (emphasis added). *See, e.g.*, *Sinorgchem Co., Shandong v. Int'l Trade Comm'n*, 511 F.3d 1132, 1136 (Fed. Cir. 2007) ("[T]he word 'is' ... may signify that a patentee is serving as its own lexicographer.") (citation and internal quotation marks omitted); *Medimmune, LLC v. PDL Biopharma, Inc.*, No. C 08–05590, 2010 WL 653546, at *6 (N.D. Cal. Feb. 22, 2010) ("It is undisputed that the specification expressly defines acceptor: 'the human immunoglobulin providing the framework is called the 'acceptor.'");

[2] Defendants believed that their construction was clear that the "electrodes" referred to in it are the pixel electrodes, as illustrated by element 20a in Fig. 6 of the '338 patent. Because Solas professes confusion in its brief, Dkt. 74 at 11-2, Defendants clarify that the topmost layer of the transistor array substrate is the layer on which the pixel electrodes are formed.

TriStrata, Inc. v. Microsoft Corp., 594 Fed. App'x 653 (Fed. Cir. Dec. 4, 2014) (unpublished); *Alacritech, Inc. v. Century Link Comm'ns LLC*, 271 F. Supp. 3d 850, 868 (E.D. Tex. 2017).

Next, the specification explains that "[t]he plurality of sub-pixel electrodes 20a are arrayed in a matrix on the upper surface of the planarization film 33, ***i.e., the upper surface of the transistor array substrate 50***." Ex. 1 ('338 patent) at 11:50-53 (emphasis added). *See Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1334 (Fed. Cir. 2009) ("the specification's use of 'i.e.' signals an intent to define the word to which it refers"). This passage again conveys that the surface on which the pixel electrodes are formed consitutes the upper surface of the transistor array substrate. Indeed, the phrasing of this passage parallels the claim language stating that the pixel electrodes are arrayed on the surface of the transistor array substrate, reinforcing that this passage is describing the claimed invention.

Thus, the claim language and specification both define the top layer of the transistor array substrate as the layer on whose upper surface the pixel electrodes are formed. The specification is clear that all of the layers beneath that layer are also part of the transistor array substrate, as illustrated in annotated Figure 6 of the patent below. *See, e.g.*, Ex. 1 ('338 patent) at 10:45-47 ("The layered structure from the insulating substrate 2 to the planarization film 33 ***is called*** a transistor array substrate 50.") (emphasis added).

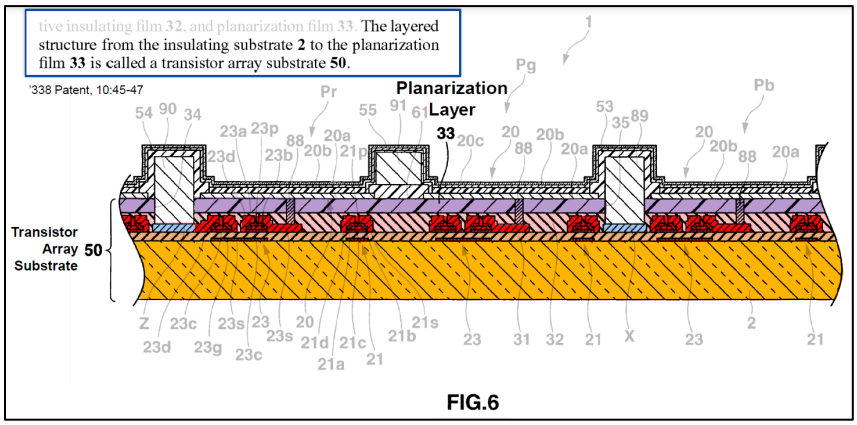

FIG.6

Defendants' proposal clarifies that the bottom-most layer is the insulating substrate, consistent with the disclosures of the '338 patent. *E.g.*, *id.* at 8:21-23 ("The display panel 1 is formed by stacking various kinds of layers on the insulating substrate 2 which is optically transparent."). Solas's contention that the bottom layer need not be insulating, Dkt. 74 at 11, is unsupported (including by its own expert) and at odds with the specification. In any event, the key point is that the "transistor array substrate" constitutes the bottom-most layer of the display panel through the layer on the surface of which pixel electrodes are formed; while that bottom-most layer will be an insulating layer, identifying it as such is not central to the claim construction dispute.

[redacted] The intrinsic evidence has not changed, only [redacted] Solas's new position is inconsistent with both the language of claim 1 and the specification. The transistor array substrate includes all layers beneath the pixel electrodes.

Solas attempts to argue that Defendants' construction would exclude a disclosed embodiment, but that is incorrect. Dkt. 74 at 11. Solas refers to an alternative embodiment having a "reflecting film" between the pixel electrode and planarization film. *Id.* (citing Ex. 1 at 11:66-12:5). Solas disregards, however, that the reflecting film would constitute a portion of the transistor array substrate, as it is the layer on which pixel electrodes are formed in that design. Thus, Defendants' construction encompasses this alternative, illustrating that it comports with all embodiments and disclosures of the specification, and does not exclude any disclosed embodiments. In contrast, under Solas's proposal there would be no way to determine whether such a reflecting film is part of the transistor array substrate or not.

Solas also asserts that the boundary of the "transistor array substrate" cannot be defined by the pixel electrodes because the specification also describes an insulating line 61 as being formed on the suface of the planarization film 33 (in a region where the pixel electrodes are not present). Dkt. 74 at 10. This is a non-sequitur. The fact that an optional insulating line 61 may also be on another portion of the surface of the transistor array substrate does not take away from the fact that the specification defines the upper surface of the transistor array substrate as the layer on which the pixel electrodes are formed. The claim language itself identifies the pixel electrodes as being formed on the surface of the transistor array substrate, while not mentioning an insulating line. Indeed, the pixel electrodes—unlike insulating line 61—are essential to the display's operation.

In contrast to the clarity provided by Defendants' construction, Solas's construction—"layered structure upon which or within which a transistor array is fabricated"—fails to indicate which layers are part of that structure and which are not, and would render the claims indefinite. Indeed, Solas's expert acknowledged in deposition that, under Solas's proposal, multiple different combinations of layers in a single device could alternatively be considered to be a "transistor array

substrate." Ex. 3 (Flasck Depo.) at 69:3-11 ("I have seen people consider this whole assembly from the bottom of 2 to the top of – whatever it is; 55, 53 – to be a transistor array substrate, and that – that whole thing could fall within the construction that we have here"), 104:4-105:3.

Moreover, Solas's expert's testimony demonstrates that Solas's construction contradicts the specification's disclosures. Solas's expert testified that, under Solas's proposal, in a device having the structure shown in Figure 6 of the '338 patent, the transistor array substrate "could" be considered to be layers 2 through 32. Ex. 3 (Flasck Depo.) at 105:4-21 ("I believe the bottom of layer 2 to the top of layer 32 could be considered a transistor array substrate as [Solas's] proposed construction states"). In other words, applying Solas's construction, the transistor array substrate may not include planarization film 33. The specification, however, explicitly identifies planarization film 33—which is on top of layer 32—as being within the transistor array substrate. *See* Ex. 1 ('338 patent) at 10: 45-47, 11:50-53. This is a crucial failing in Solas's construction, particularly given that the patent claims define other structures by reference to the surface of the transistor array substrate: the interconnections "project from" a surface of the transistor array substrate, and the pixel electrodes are "on the surface of the transistor array substrate."

Under Solas's proposal, there is not even a basis to include within the transistor array substrate numerous layers that the specification expressly identifies as portions of the transistor array substrate. For instance, planarization layer 33 is neither beneath the array of transistors nor a layer that contains transistors. Yet, the '338 patent is explicit that planarization layer 33 *is* part of the claimed "transistor array substrate." Ex. 1 at 11:50-53.

Notably, Solas criticizes Defendants' proposal on the ground that it would create ambiguity in what layers constitute the transistor array substrate, based on the incorrect premise that the "electrode" in Defendants' proposal could be any electrode, and not the pixel electrode (as

Defendants had intended and thought was clear). Dkt. 74 at 11-12. Solas is wrong, because Defendants' proposal refers to the pixel electrode. *See supra* at n.2. Yet Solas's argument highlights a fundamental failing in Solas's construction: it provides no basis to determine whether particular layers of a device are within or outside the "transistor array substrate," and as a result the scope of the claim could not be ascertained with reasonable certainty. A factfinder would have no way of determining under Solas's construction whether a given set of layers are properly considered to be part of the transistor array substrate or not.

Thus, consistent with all of the intrinsic evidence, "transistor array substrate" should be construed as "a layered structure composed of a bottom insulating layer through a topmost layer on whose upper surface [pixel] electrodes are formed, which contains an array of transistors."

2. "project from a surface of the transistor array substrate" (claim 1)

Defendants' Proposal	**Plaintiff's Proposal**
"extend above the upper surface of the transistor array substrate"	"extend from a surface of the transistor array substrate"

Claim 1 states that the claimed display panel comprises "a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other." The parties' dispute centers on whether this means that the interconnections extend beyond the boundary of the transistor array substrate, as Defendants propose and the '338 patent describes, or whether the interconnections may be fully embedded within the transistor array substrate, as Solas proposes. The plain meaning of the claim language and the disclosures of the specification all support Defendants' proposal.

Although Solas's brief obscures the true dispute between the parties, Solas's expert revealed it in his deposition. He testified that materials that are fully embedded within the transistor array substrate—that do not in any way extend outside the transistor array substrate—would, under Solas's proposal, be said to "project from" a surface of the transistor array substrate.

See, e.g., Ex. 3 (Flasck Depo.) at 35:17-22 ("Various parts of [transistor] 23 do project from a surface of the transistor array substrate"); 37:21-38:4 ("[Gate insulating] [l]ayer 31 does project from a surface of the transistor array substrate"); 45:15-20; 53:12-54:19; 55:1-10; 74:2-25.

Solas takes this position, which flies in the face of the claim language, by (1) incorrectly treating interfaces between sublayers *inside* the transistor array substrate as being "a surface" of the transistor array substrate, and then (2) positing that an interconnection extending in any direction beyond any such interface purportedly "projects from" the "surface." In other words, Solas takes the position that the top, bottom, and sides of any *sublayer* of the transistor array substrate constitutes a "surface" of the transistor array substrate, and an interconnection that extends in any way above or below or to the side "projects from" a "surface" of the transistor array substrate. What this means is that, under Solas's proposal, *any* interconnection would *necessarily* project from a surface of the transistor array substrate. It would be impossible, under Solas's proposal, for there to exist an interconnection that did not "project from" some "surface" of the transistor array substrate. Solas's construction effectively reads the "projects from" limitation out of the claim through its use of the term "a surface." This is improper. *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006) ("claims are interpreted with an eye toward giving effect to all terms in the claim").

Solas identifies no support in the written description or figures of the '338 patent for its position that an interconnection that "projects from a surface of the transistor array substrate" but is fully embedded inside the transistor array substrate. There is no such support. On the contrary, Solas's construction is belied by the claim language and the specification.

The plain meaning of the claim language "interconnections which are formed to project from a surface of the transistor array substrate" is that the interconnections extend outside the

transistor array substrate. The plain meaning alone requires rejection of Solas's position that the interconnections can be entirely embedded within the transistor array substrate.

Further, the specification strongly supports Defendants' construction. Consistent with the plain meaning of "projects from," the specification explains that the interconnections extend beyond the upper surface of the transistor array substrate. The specification explains "[t]he common interconnection 91 is formed by electroplating and is therefore formed to be much thicker than the signal line Y, scan line X, and supply line Z and ***project upward from the surface*** of the planarization film 33." Ex. 1 ('338 patent) at 10:54-58 (emphasis added). The specification then explains that "[t]he thickness of the select interconnection 89 and feed interconnection 90 is larger than the total thickness of the protective insulating film 32 and planarization film 33 so that the select interconnection 89 and feed interconnection 90 ***project upward from the upper surface*** of the planarization film 33." *Id.* at 11:36-41 (emphasis added). The specification also makes clear that the upper surface of the planarization film is the upper surface of the transistor array substrate. *See, e.g.*, *id.* at 10:49-50 ("the upper surface of the planarization film 33, ***i.e.***, the upper surface of the transistor array substrate 50") (emphasis added); 11:50-52 (same); 10:45-47.

Defendants' proposal also aligns with the purpose of the interconnections projecting from a surface of the transistor array substrate. The '338 patent repeatedly explains that the projecting interconnections "serve as partition walls to prevent leakage of an organic compound-containing solution." Ex. 1 ('338 patent) at 6:24-30*; see also id.* at 6:38-42. To serve as these partition walls, the interconnections must extend past the upper surface of the transistor array substrate. This is precisely what the specification of the '338 patent describes and its Figures illustrate: all interconnections (89, 90, and 91 in Figure 6) extend above the upper surface (33) of the transistor array substrate:

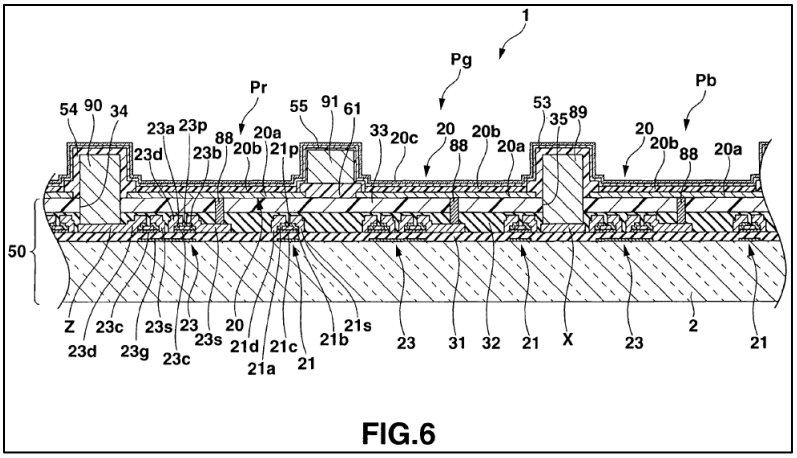

FIG.6

In fact, in language that parallels the claim language, the specification explains that projecting interconnections extend above the upper surface of the transistor array substrate to prevent leakage of the organic electroluminescent compound: "[t]he thick select interconnection 89, feed interconnection 90, and common interconnection 91 whose tops are much higher than that of the insulating line 61 *are formed* between the sub-pixel electrodes 20a adjacent in the vertical direction ***to project respect to the surface of the transistor array substrate 50***. ***Hence, the organic compound-containing solution*** applied to a sub-pixel electrode 20a ***is prevented from leaking*** to the sub-pixel electrodes 20a adjacent in the vertical direction." *Id.* at 12:62-13:3 (emphases added). The specification further explains that "[s]ince the select interconnections 89, feed interconnections 90, and common interconnections 91 ***formed to project*** are provided thick, the organic EL layers 20b can have different colors by wet coating" while "no special banks to partition the sub-pixels P need be provided…." *Id.* at 22:62-66 (emphasis added). These disclosures reiterate that the interconnections extend above the upper surface of the transistor array substrate, as Defendants propose.

Not only does Solas's construction contradict the claim language and clear disclosures of the specification, it is belied by [redacted] In fact, [redacted]

[redacted]

[redacted]

[redacted]

[redacted] Solas makes no effort to reconcile its current position, and its criticisms of Defendants' construction, with the fact that [redacted] The intrinsic evidence has not changed.

Thus, the plain meaning of the claim language and the disclosures of the specification support Defendants' construction.

3. "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate" (claim 1)

Defendants' Proposal	Plaintiff's Proposal
"the pixel electrodes are arrayed along the interconnections and located between the interconnections, and the pixel electrodes are on the surface of the transistor array substrate"	"the pixel electrodes are arrayed along the interconnections and located between the interconnections that are on the surface of the transistor array substrate"

Defendants' proposed construction represents the plain meaning of the claim language. This is apparent from the surrounding claim language. Immediately preceding the disputed phrase, the claim recites that the display panel comprises "a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed parallel to each other." Ex. 1 ('338 patent) at 24:19-22. Thus, the claim language first describes the position of the interconnections with respect to the transistor array substrate. The claim next recites that the display panel also contains "a plurality of pixel electrodes" and describes the position of the pixel electrodes: "the pixel electrodes being arrayed [1] along the interconnections between the interconnections [2] on the surface of the transistor array substrate." *Id.* at 22:26. Thus, the pixel electrodes are on the surface of the transistor array substrate and arrayed (i.e., located) along and between the parallel interconnections. The natural reading of the claim structure is that after describing the location of the interconnections with respect to the transistor array substrate, the claim proceeds to describe the location of the pixel electrodes with respect to the interconnections (along and between them) and with respect to the transistor array substrate (on the surface of it).

To the extent there is ambiguity in the claim language, the specification resolves it, establishing that Defendants' interpretation is the correct one. *See Phillips*, 415 F.3d at 1315 ("[C]laims must be read in view of the specification," which "is the single best guide to the

meaning of a disputed term"). The specification explains the pixel electrodes run in parallel to the interconnections, are located between them, and are on the surface of the transistor array substrate.

The specification first explains, and illustrates in Figures 3-5, that the pixel electrodes are arrayed along the interconnections between the interconnections. *See, e.g.*, Ex. 1 ('338 patent) at 5:57-6:2 ("the plurality of sub-pixel electrodes 20a are arrayed in the horizontal direction between the feed interconnection 90 and the adjacent common interconnection 91," "between the common interconnection 91 and the adjacent select interconnection 89," and "between the select interconnection 89 and the adjacent feed interconnection 90."); *id.* at 12:31-54.

The specification next explains, and illustrates in Figure 6, that the pixel electrodes are on the surface of the transistor array substrate. The specification explicitly states that "[t]he plurality of sub-pixel electrodes 20a are arrayed in a matrix ***on the upper surface of the planarization film 33, i.e., the upper surface of the transistor array substrate 50.***" *Id.* at 11:50-52 (emphasis added). *Edwards Lifesciences*, 582 F.3d at 1334 ("the specification's use of 'i.e.' signals an intent to define the word to which it refers"). And Figure 6 shows that the pixel electrodes (20a) are on the surface of the transistor array substrate (50). Thus, both the claim language and the clear teachings of the specification support Defendants' proposed construction.

In contrast, there is no description in the specification supporting Solas's construction, nor any support for it in the '338 patent's figures. On the contrary, Solas's construction is inconsistent with the claim language and contrary to the disclosures of the specification. Solas's proposal—that it is the interconnections that must be "on the surface of the transistor array substrate"—would exclude a preferred embodiment, as the specification discloses that "common interconnection 91" is ***not*** on the surface of the transistor array substrate. Rather, as shown in Figure 6, "[t]he common interconnection 91 . . . is formed on the insulating line 61," Ex. 1 ('338 patent) at 10:52-54, which

is not part of the transistor array substrate but rather a separate structure that itself is formed on the surface of the transistor array substrate, *see id.* at 10:48-54 ("An insulating line 61 . . . is formed on the surface of the planarization film 33, i.e., on the surface of the transistor array substrate 50"). A claim construction that, like Solas's, excludes the preferred embodiment is "rarely, if ever, correct and would require highly persuasive evidentiary support." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996).

Solas attempts to deflect from this defect in its position by arguing that interconnection 91 is "on" the transistor array substrate because it is above it. But Solas bases its argument on a false premise: the claim language does not use the term "on," it refers to a structure "***on the surface of***" the transistor array substrate. The specification is clear that interconnection 91 is ***not*** "on the surface of" the transistor array substrate, but rather "on the surface of" another structure. *See supra*. By contrast, the specification is explicit that the pixel electrodes are on the surface of the transistor array substrate (as Defendants propose). Ex. 1 ('338 patent) at 11:50-52; Fig. 6.

Nor is there merit to Solas's fallback argument that the claims do not require the common interconnections to be on the surface of the transistor array substrate. The '338 patent describes the structure in Figure 6 as a preferred embodiment. Ex. 1 ('338 patent) at 4:42-51, 8:18-20. In this structure, the common interconnections are not on the surface of the transistor array substrate, whereas all of the pixel electrodes are. Moreover, Solas's argument is belied by dependent claim 2, which makes clear that the "common interconnection"—element 90 in the specification and Figure 6—is among the claimed plurality of interconnections.

Solas's proposal has further fundamental defects as well. Solas's argument that the interconnections are "on the surface of the transistor array" would render superfluous the separate limitation that the interconnections "project from a surface of the transistor array substrate." If an

interconnection is "on the surface" of the transistor array substrate, then it necessarily would project from the surface of the transistor array substrate. Thus, Solas's proposal would render the limitation that the interconnections "projects from" a surface of the transistor array substrate superfluous in the claim, which is heavily disfavored. *Bicon*, 441 F.3d at 950 ("claims are interpreted with an eye toward giving effect to all terms in the claim"); *Merck*, 395 F.3d at 1372. Indeed, Solas's expert acknowledged that "something that projects from the surface is also on the surface." Ex. 3 (Flasck Depo.) at 67:14-18 (Q: "Are you saying that something that projects from a surface is also on the surface?" A: "Yes.").

In addition, there is no support in the specification for arraying the pixel electrodes on a structure other than the surface of the transistor array substrate. The specification is clear that "[t]he plurality of ***sub-pixel electrodes 20a are arrayed*** in a matrix *on the upper surface of the planarization film 33, i.e.,* ***the upper surface of the transistor array substrate 50***." Ex. 1 ('338 patent) at 11:50-52. This is shown in Figure 6. In contrast, there is no description stating, or figure showing, that a pixel electrode is not on the surface of the transistor array substrate.

Nor does the prosecution history support Solas's construction. *Contra* Dkt. 74 at 17. The applicants' February 25, 2008 amendment was described as making "minor grammatical improvements and to correct some minor antecedent basis problems." *Id*. Both the original claim language and the amended language describe the plurality of pixel electrodes, consistent with the specification, as being arrayed along and between the interconnections and formed on the surface of the transistor array substrate. *Id.* Notably, the applicants did not alter the separate limitation describing the "plurality of interconnections," which would have been the natural place to recite that the *interconnections* are formed "on the surface" of the transistor array substrate, had that been the intended meaning. Rather, the structure of the claim supports Defendants' construction.

[redacted] Again, the intrinsic evidence has not changed since [redacted]

4. "write current" (claim 1)

Defendants' Proposal	Plaintiff's Proposal
"pull-out current"	No construction required

The parties appear to agree that the '338 patent discloses the use of a current, known as a write current, to determine the brightness of an individual pixel in the display rather than relying on a voltage signal. The '338 patent defines the "write current" as "pull-out current," as Defendants propose. Defendants' construction provides the term the meaning it clearly has in the '338 patent, and would assist the jury by clarifying what is meant by a write current.

The '338 patent repeatedly and consistently defines "write current" as "pull-out current." The specification equates "write current" with "pull-out current" no fewer than ***eighteen times***:

- *See* Ex. 1 ('338 patent) at 15:34-37 ("As shown in FIG. 2, a ***write current (pull-out current)*** having a current value corresponding to the gray level is supplied from the data driver to the signal lines.");
- 15:37-41 ("[T]he ***write current (pull-out current)*** to the signal line Y_j flows from the feed interconnection 90 and supply line Z_i through the drain-to-source path of the driving transistor 23 and the drain-to-source path of the switch transistor 21.");
- 15:43-45 ("The data driver sets the current value of the ***write current (pull-out current)*** in accordance with an externally input gray level.");

- 15:45-54 ("While the ***write current (pull-out current)*** is flowing, the voltage between the gate 23g and source 23s of the driving transistor 23 of each of pixel circuits $P_{i,1}$ to $P_{i,n}$ of the ith row is forcibly set in accordance with the current value of the ***write current (pull-out current)*** flowing to the signal lines Y_1 to Y_n, i.e., the current value of the ***write current (pull-out current)*** flowing between the drain 23d and source 23s of the driving transistor 23 independently of the change over time in the Vg-Ids characteristic of the driving transistor 23);

- 15:54-58 ("Charges with a magnitude corresponding to the level of this voltage are stored in the capacitor 24 so that the current value of the ***write current (pull-out current)*** is converted into the voltage level between the gate 23g and source 23s of the driving transistor 23.");

- 16:11-13 ("[T]he current value of the driving current in the light emission period equals the current value of the ***write current (pull-out current)*** in the selection period.");

- 16:38-41 ("[A] ***write current (pull-out current)*** having a current value corresponding to the gray level is supplied from the data driver to the signal lines Y_1 to Y_n, as indicated by the arrow A.");

- 16:42-46 ("[T]he ***write current (pull-out current)*** to the signal line Y_j flows from the feed interconnection 90 and supply line Z_i through the drain-to-source path of the driving transistor 23 and the drain-to-source path of the switch transistor 21.");

- 16:48-50 ("The data driver sets the current value of the ***write current (pull-out current)*** in accordance with an externally input gray level.");

- 16:50-59 ("While the ***write current (pull-out current)*** is flowing, the voltage between the gate 23g and source 23s of the driving transistor 23 of each of the pixel circuits $P_{i,1}$ to $P_{i,n}$ of the ith row is forcibly set in accordance with the current value of the ***write current (pull-out current)*** flowing to the signal lines Y_1 to Y_n, i.e., the current value of the ***write current (pull-out current)*** flowing between the drain 23d and source 23s of the driving transistor 23 independently of the change over time in the Vg-Ids characteristic of the transistor 23.");

- 16:59-63 ("Charges with a magnitude corresponding to the level of this voltage are stored in the capacitor 24 so that the current value of the ***write current (pull-out current)*** is converted into the voltage level between the gate 23g and source 23s.");

- 17:17-19 ("[T]he current value of the driving current in the light emission period equals the current value of ***the write current (pull-out current)*** in the selection period.");

- 17:53-55 ("***[T]he write current (pull-out current)*** can sufficiently be supplied without any delay.");

- 17:59-62 ("[T]he magnitude of the driving current flowing to the common interconnection 91 in the light emission period equals that ***of the write current (pull-out current)*** flowing to the feed interconnection 90 in the selection period.").

(emphases added). Solas's characterization of the specification as equating write current with pull-out current in "several instances," Dkt. 74 at 22, is simply not accurate.

Figure 2, shown below with annotations, specifically illustrates that "write current" is pull-out current. The specification also emphasizes this in its text, stating that "[a]s shown in FIG. 2, ***a write current (pull-out current***) having a current value corresponding to the gray level is supplied from the data driver to the signal lines Y_1 to Y_n, ***as indicated by an arrow A***." Ex. 1 ('338 patent) at 15:34-37 (emphases added). In fact, the applicants specifically cited Figure 2, along with a passage from the specification equating write current with pull-out current, when they added the claim language about "write current" to claim 1. *See* Ex. 2 (February 25, 2008 Amendment) at 12. These were the *only* materials the applicants cited to explain the write current.

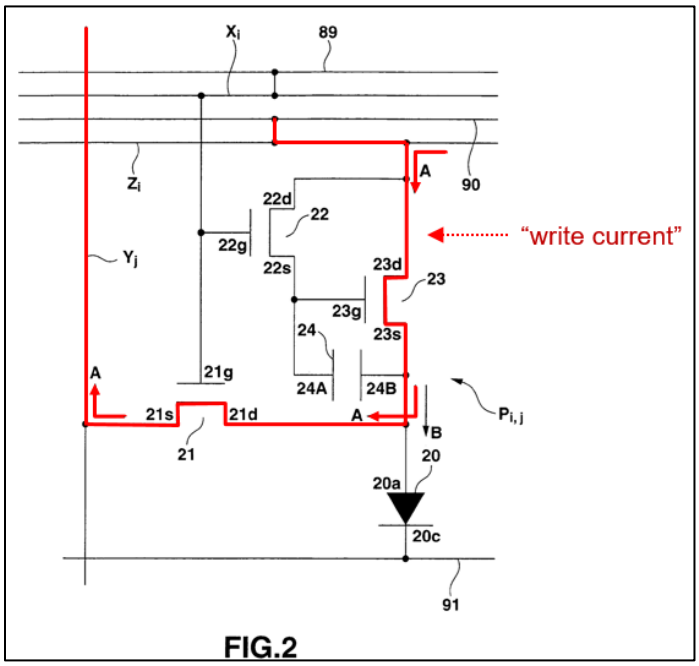

FIG.2

There is no apparent dispute that, in the operation of the devices disclosed in the '338 patent, write current is pull-out current. Solas's expert, in deposition, conceded that the "write

current" in the '338 patent flows through transistors 21 and 23 "to the signal line Yi" due to what he termed a "current sink attached to Yi," Ex. 3 (Flasck Depo.) at 21:15-22:4, and explained that the "current sink . . . pulls in a given current level" out of the circuit, *id.* at 22:6-23:5. Thus, the meaning of the write current in the '338 patent is clear, and it is pull-out current.

Further, there is no disclosure in the '338 patent of write current that is not pull-out current. Although Solas asserts that "there are other disclosures that use different words in parentheses following 'write current,'" Dkt. 74 at 24 (emphases omitted), citing just two passages, both passages in fact describe pull-out current. When the specification states "write current (current signal)," Ex. 1 ('338 patent) at 14:60-61, it is describing the pull-out current in Figure 2; the specification confirms that "current signal" is synonymous with a "pull-out current" by later equating those terms, *see id.* at 16:24-25 ("pull-out current (current signal)"). As to column 17, line 47 of the '338 patent ("write current (driving current)"), in that sentence, the specification is simply explaining that the *magnitude* of write current in the selection period equals the magnitude of driving current in the subsequent light emission period; importantly, in the same paragraph, just two sentences later, the specification reiterates that write current is pull-out current. *See id.* at 17:44-55. Solas disregards this context.

Not only does the specification consistently define the write current as pull-out current, the specification does so in multiple passages that use the phrasing "i.e.," reinforcing that those passages are intended to be definitional statements. *Edwards Lifesciences*, 582 F.3d at 1334 ("the specification's use of 'i.e.' signals an intent to define the word to which it refers"). For instance, the specification twice states that:

> While the write current (pull-out current) is flowing, the voltage between the gate 23g and source 23s of the driving transistor 23 of each of pixel circuits … is forcibly set in accordance with the current value of the write current (pull-out current) flowing to the signal

> lines Yi to Yn ***i.e.***, the current value ***of the write current (pull-out current)*** flowing between the drain 23d and source 23s of the driving transistor 23 independently of the change over time in the Vg-Ids characteristic of the driving transistor 23.

Ex. 1 ('338 patent) at 15:45-54 (emphases added); 16:50-59 (same).

The definition of the "write current" as pull-out current is not merely an aspect of a preferred embodiment, it is a foundational feature of the '338 patent's circuit structure. During prosecution, the applicants added the language concerning the circuit structure to claim 1 from a dependent claim, to overcome a prior art rejection. Ex. 2 at 2-3, 12. When the applicants did so, they specifically revised the claim language about "write current." *Id.* The applicants' change to this claim language further bolsters Defendants' construction and contradicts Solas's position.

The applicants explained in amending claim 1 during prosecution that "the phrase 'a switch transistor *which supplies a write current*' in original [prosecution] claim 2 has been ***changed*** to 'a switch transistor *which makes a write current flow*." *Id.* at 12 (emphasis added). In support of the amendment, the applicants specifically cited "Fig. 2 and page 41, lines 20-25 of the specification," *id.*, each of which discloses that the "write current" refers to pull-out current. As discussed above, Figure 2 depicts the pull-out current, which is marked as "A." The passage at page 41, lines 20-25 (which corresponds to Col. 15:37-41 of the issued patent) explicitly equates write current with pull-out current: "In the pixel circuit, $P_{i,j}$, ***the write current (pull-out current)*** to the signal line Y_j flows from the feed interconnection 90 and supply line Z_i through the drain-to-source path of the driving transistor 23 and the drain-to-source path of the switch transistor 21." Ex. 8 (September 26, 2005 original specification) at 41:20-25 (emphasis added). Thus, the very portion of the specification that the applicants called out to support their amended claim language explicitly provides that write current refers to pull-out current. In fact, the sentences immediately following

in the specification elaborate on this and further reinforce that the "write current" is a pull-out current. Ex. 1 ('338 patent) at 15:42-54 (repeatedly reciting "write current (pull-out current)").

Although Solas asserts that "write current" has a plain meaning outside the context of the '338 patent, Dkt. 74 at 20, it is revealing that Solas provides no support, failing to cite a single supporting reference, dictionary, or treatise. Solas offers just the *ipse dixit* of its expert, which is not grounds to disregard the intrinsic evidence. *Phillips*, 415 F.3d at 1318 ("[C]onclusory, unsupported assertions by experts as to the definition of a claim term are not useful to a court").

Moreover, Solas's brief and expert declaration suggest that Solas is attempting to undo the amendment the applicants made during prosecution, and to return to language the applicants disavowed. The applicants made clear that they were changing the claim language so as *not* to recite "a switch transistor *which supplies a write current*." Yet Solas's expert declaration asserts, without acknowledging the prosecution history, that a write current should be interpreted as "a current *that is supplied* from outside of the pixel circuit (for example via a signal line) and is used to 'write' information … that is stored in the pixel circuit." Dkt. 74-2 (Flasck Decl.) at ¶ 61. An expert may not contradict the intrinsic evidence. *Phillips*, 415 F.3d at 1318 ("[A] court should discount any expert testimony 'that is clearly at odds with [the intrinsic evidence]'").

Finally, to the extent that Solas contends "write current" in the '338 patent can mean something different than pull-out current, Solas fails to present any construction that would inform the factfinder what else it means. Solas cannot argue that no construction is required when it takes the position that "write current" does not mean what is described in the specification and prosecution history of the '338 patent. Given the dispute over the meaning of the term, it is necessary to assign a meaning to "write current." The definition provided in the '338 patent and its prosecution history, that write current is pull-out current, provides that meaning.

C. Background of the '311 Patent

The application that led to the '311 patent underwent numerous rounds of rejections and claim amendments over nearly four years of prosecution before narrowed claims were ultimately allowed. The originally filed claims were directed to "a substantially flexible substrate" and "touch sensor disposed on the substantially flexible substrate" without any recitation of an "edge" or wrapping around an edge, and were rejected as obvious. *See* Ex. 9 (excerpts from '311 patent file history) at 168-169 (October 2011 Original Claims); *id.* at 138-153 (2013 Office Action). After further rounds of amendments and rejections, *see, e.g.*, *id.* at 96-107 (2014 Amendment); 39-48 (2015 Amendment), *id.* at 21-38 (2015 Non-Final Rejection), the claims were allowed after the applicants added a new limitation to each independent claim reciting, based on one set of embodiments in the specification, that "the substantially flexible substrate and the touch sensor are configured to wrap around one or more edges of a display," *id.* at 11-12 (June 2015 Amendment). Figure 7 exemplifies that set of embodiments, showing "touch-sensitive apparatus 612 wrapped around an example display 613." Ex. 10 ('311 patent) at 7:39-41.

D. Disputed Term of the '311 Patent[3]

1. "configured to wrap around one or more edges of a display" (claims 1 and 7)

Defendants' Proposal	Plaintiff's Proposal
"wrapped around one or more line segments where two surfaces of a display intersect"	No construction required

Defendants' proposed construction is the plain meaning of the claim language in the art of the '311 patent. The term "edge" has a plain and ordinary meaning in a technical context when referring to three-dimensional objects. It refers to a line where two surfaces intersect. *See, e.g.*,

[3] A person of ordinary skill in the art of the '311 patent would have had a relevant technical degree in Electrical Engineering, Computer Engineering, Computer Science, Materials Science, or the like, and 2–3 years of experience in touch sensor design.

Ex. 11 ("Concise Oxford English Dictionary," Oxford University Press (12th ed. 2011)) at 455 ("edge": "the line along which two surfaces of a solid meet"); Ex. 12 ("McGraw-Hill Dictionary of Scientific and Technical Terms (5th ed. 1994)) at 641 ("edge": "a line along which two plane faces of a solid intersect"). This contrasts with the definition of "edge" when referring to two-dimensional objects, where it may refer to a side. *See, e.g.*, Ex. 13 (Dictionary of Computing (6th ed. 2010)) at 119 ("edge": "a side of a flat object").

In the '311 patent, the term "edge" is necessarily being used in the context of three-dimensional structures, as the claim language requires that "the substantially flexible substrate and the touch sensor" be configured to "*wrap around* one or more edges of the display." Ex. 10 ('311 patent), 9:5-7. To "wrap around" the edge, the structure must be three-dimensional. Consistent with the plain meaning, Figure 7 shows a touch sensor (annotated below in blue) wrapping around a line segment where two surfaces of the display (annotated in yellow) meet.

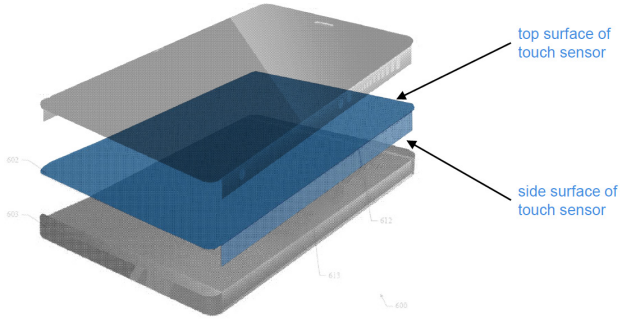

Figure 7

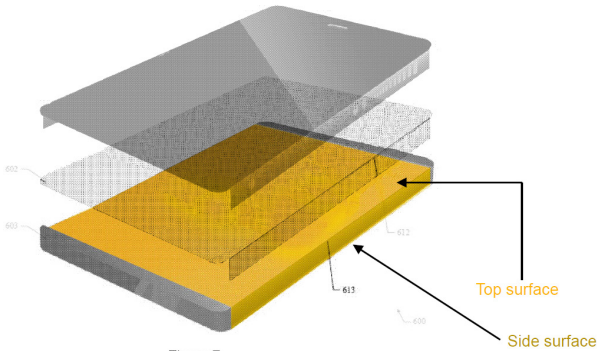

Figure 7

The specification shows that the term "edge" is used in the '311 patent consistent with its ordinary meaning in technical contexts. The specification states that "Substrate 602 and the conductive material of the electrode pattern may be flexible, enabling the conductive material to wrap around *the left and right edges of the surface to left-side and right-side surfaces*." *Id.* at 7:48-51 (emphasis added). In other words, the left edge of the horizontal surface is where the surface intersects with the left-side vertical surface.

Consistent with this plain meaning, the specification also draws a distinction between two types of embodiments: one set of embodiments in which the touch-sensitive apparatus "may wrap around an *edge*" and a separate set of embodiments in which the touch-sensitive apparatus "may be wrapped around a curved surface." *Id.* at 7:55-58. The specification explains that "***[i]n particular embodiments***, the electrode pattern ***may wrap around an edge*** 603 of example mobile phone 600. ***In other particular embodiments***, touch-sensitive apparatus 612 ***may be wrapped around a curved surface***." *Id.* (emphases added). Thus, consistent with the plain and ordinary meaning of "edge," the '311 patent makes clear that "a curved surface" is different from an edge.

The applicants added the "wrap around an edge" limitation during prosecution to overcome repeated rejections of broader prosecution claims (*see* Ex. 9 at 10-20) that had also encompassed the separate set of embodiments in which touch sensors were configured to wrap around "a curved surface," Ex. 10 ('311 patent), at 7:55-58. To secure the claims, the applicants elected to claim one of the types of embodiments disclosed ("wrap[ped] around an edge") and not the other ("wrapped around curved surface"). Solas cannot now contend that the allowed '311 patent claims cover such embodiments.

Further, contrary to Solas's assertion, Defendants did not "acknowledge[] to the Patent Trial and Appeal Board that the phrases [sic] 'edges of a display' could cover" both of "these two types of embodiments." Dkt. 74 at 30. Solas has inserted highlighting and italics into an excerpt from Defendants' IPR petition to insinuate that the phrase "It describes" meant "An edge of a display describes," but that is incorrect. The pronoun "It" in "It describes" refers to "the '311 patent"; the passage was explaining the distinction *the patent* draws in its specification between the "particular embodiments" in which the touch sensor wraps around an edge of a device, and the "other particular embodiments" in which the touch sensor is wrapped around a curved surface, *see*

id., just as discussed above. The claims, however, were narrowed after the repeated rejections to be directed to one set of embodiments, i.e., those in which the touch sensor wraps around an edge.

Finally, Defendants' construction does not limit the claim to "sharper edges," contrary to Solas's assertion. The '311 patent notes that an edge may be sharper, e.g., "with radii of less than 1 mm," or, by implication, less sharp. Ex. 10 ('311 patent) at 7:52-55. However, the fact that an edge may be less sharp does not effectively remove the "edge" limitation from the claim. A rounded edge differs from a curved surface in that it joins two distinct surfaces.

Thus, Defendants' construction represents the plain and ordinary meaning of "edge," as found in dictionaries and consistent with the '311 patent's specification. Insofar as Solas contests this definition, it cannot contend that no construction is required. Not only has Solas failed to indicate what specialized meaning it seeks to attribute to the term, it has wholly failed to support doing so.

IV. CONCLUSION

For the above reasons, Defendants respectfully request that the Court adopt their proposed claim constructions.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of the foregoing document via the Court's CM/ECF system per Local Rule CV-5(a)(3) this March 4, 2020.

/s/ Melissa R. Smith
Melissa R. Smith

[redacted]